

MAXIM

10-Bit Voltage-Output DAC in 8-Pin μ MAX

MAX5304

General Description

The MAX5304 combines a low-power, voltage-output, 10-bit digital-to-analog converter (DAC) and a precision output amplifier in an 8-pin μ MAX package. It operates from a single +5V supply, drawing less than 280 μ A of supply current.

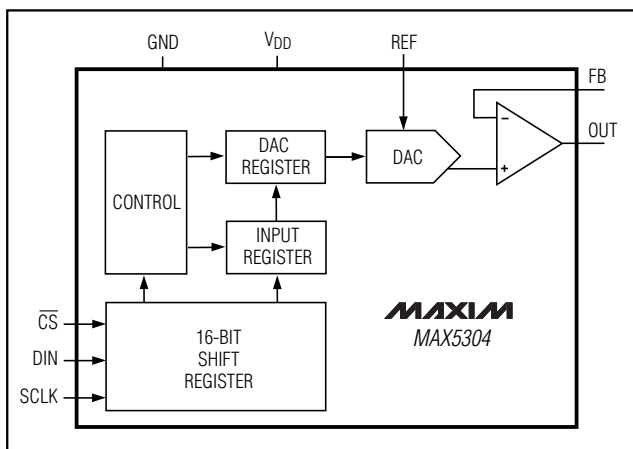
The output amplifier's inverting input is available to the user, allowing specific gain configurations, remote sensing, and high output-current capability. This makes the MAX5304 ideal for a wide range of applications, including industrial process control. Other features include a software shutdown and power-on reset.

The serial interface is SPI™/QSPI™/MICROWIRE™ compatible. The DAC has a double-buffered input, organized as an input register followed by a DAC register. A 16-bit serial word loads data into the input register. The DAC register can be updated independently or simultaneously with the input register. All logic inputs are TTL/CMOS-logic compatible and buffered with Schmitt triggers to allow direct interfacing to optocouplers.

Applications

Digital Offset and Gain Adjustment
Industrial Process Control
Microprocessor-Controlled Systems
Portable Test Instruments
Remote Industrial Control

Functional Diagram



SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

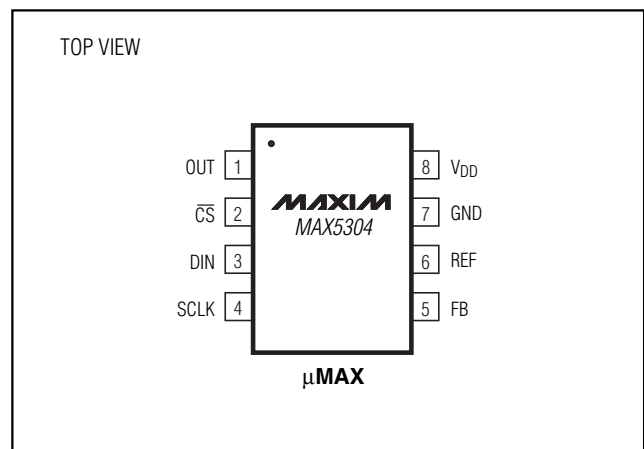
Features

- ◆ 10-Bit DAC with Configurable Output Amplifier
- ◆ +5V Single-Supply Operation
- ◆ Low Supply Current
 - 0.28mA Normal Operation
 - 2 μ A Shutdown Mode
- ◆ Available in 8-Pin μ MAX
- ◆ Power-On Reset Clears DAC Output to Zero
- ◆ SPI/QSPI/MICROWIRE Compatible
- ◆ Schmitt-Trigger Digital Inputs for Direct Optocoupler Interface

Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
|------------|----------------|-------------|
| MAX5304CUA | 0°C to +70°C | 8 μ MAX |
| MAX5304EUA | -40°C to +85°C | 8 μ MAX |

Pin Configuration



10-Bit Voltage-Output DAC in 8-Pin μ MAX

ABSOLUTE MAXIMUM RATINGS

| | |
|--|------------------------------|
| V_{DD} to GND..... | -0.3V to +6V |
| REF, OUT, FB to GND..... | -0.3V to ($V_{DD} + 0.3V$) |
| Digital Inputs to GND..... | -0.3V to +6V |
| Continuous Current into Any Pin..... | $\pm 20mA$ |
| Continuous Power Dissipation ($T_A = +70^\circ C$) 8-Pin μ MAX (derate 4.10mW/ $^\circ C$ above +70 $^\circ C$)..... | 330mW |

| | |
|--|-----------------------------------|
| Operating Temperature Ranges | |
| MAX5304CUA..... | 0 $^\circ C$ to +70 $^\circ C$ |
| MAX5304EUA..... | -40 $^\circ C$ to +85 $^\circ C$ |
| Junction Temperature..... | +150 $^\circ C$ |
| Storage Temperature Range..... | -65 $^\circ C$ to +150 $^\circ C$ |
| Lead Temperature (soldering, 10s)..... | +300 $^\circ C$ |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 8, $V_{DD} = +5V \pm 10\%$, $V_{REF} = +2.5V$, $R_L = 5k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$. Output buffer connected in unity-gain configuration.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------|---|-----|-----------|----------------|-----------------|
| STATIC PERFORMANCE—ANALOG SECTION | | | | | | |
| Resolution | N | | 10 | | | Bits |
| Differential Nonlinearity | DNL | Guaranteed monotonic | | | ± 1.0 | LSB |
| Integral Nonlinearity (Note 1) | INL | | | | ± 4 | LSB |
| Offset Error | V_{OS} | | | ± 0.3 | ± 8 | mV |
| Offset-Error Tempco | TCV_{OS} | | | 6 | | ppm/ $^\circ C$ |
| Gain Error (Note 1) | GE | | | -0.3 | ± 2 | LSB |
| Gain-Error Tempco | | | | 1 | | ppm/ $^\circ C$ |
| Power-Supply Rejection Ratio | PSRR | $4.5V \leq V_{DD} \leq 5.5V$ | | | 800 | $\mu V/V$ |
| REFERENCE INPUT | | | | | | |
| Reference Input Range | V_{REF} | | 0 | | $V_{DD} - 1.4$ | V |
| Reference Input Resistance | R_{REF} | Code dependent, minimum at code 1550 hex | 18 | 30 | | k Ω |
| MULTIPLYING-MODE PERFORMANCE | | | | | | |
| Reference -3dB Bandwidth | | $V_{REF} = 0.67V_{p-p}$ | | 650 | | kHz |
| Reference Feedthrough | | Input code = all 0s, $V_{REF} = 3.6V_{p-p}$ at 1kHz | | -84 | | dB |
| Signal-to-Noise Plus Distortion Ratio | SINAD | $V_{REF} = 1V_{p-p}$ at 25kHz, code = full scale | | 77 | | dB |
| DIGITAL INPUTS | | | | | | |
| Input High Voltage | V_{IH} | | 2.4 | | | V |
| Input Low Voltage | V_{IL} | | | | 0.8 | V |
| Input Leakage Current | I_{IN} | $V_{IN} = 0$ or V_{DD} | | 0.001 | ± 0.5 | μA |
| Input Capacitance | C_{IN} | | | 8 | | pF |

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 8, $V_{DD} = +5V \pm 10\%$, $V_{REF} = +2.5V$, $R_L = 5k\Omega$, $C_L = 100pF$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$. Output buffer connected in unity-gain configuration.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------|---|-----|---------------|-----------|------------|
| DYNAMIC PERFORMANCE | | | | | | |
| Voltage Output Slew Rate | SR | | | 0.6 | | V/ μ s |
| Output Settling Time | | To $\pm 1/2$ LSB, $V_{STEP} = 2.5V$ | | 10 | | μ s |
| Output Voltage Swing | | Rail-to-rail (Note 2) | | 0 to V_{DD} | | V |
| Current into FB | | | | 0.001 | ± 0.1 | μ A |
| Start-Up Time | | | | 20 | | μ s |
| Digital Feedthrough | | $\overline{CS} = V_{DD}$, DIN = 100kHz | | 5 | | nVs |
| POWER SUPPLIES | | | | | | |
| Supply Voltage | V_{DD} | | 4.5 | | 5.5 | V |
| Supply Current | I_{DD} | (Note 3) | | 0.28 | 0.4 | mA |
| Supply Current in Shutdown | | (Note 3) | | 4 | 20 | μ A |
| Reference Current in Shutdown | | | | 0.001 | ± 0.5 | μ A |
| TIMING CHARACTERISTICS (Figure 6) | | | | | | |
| SCLK Clock Period | tCP | | 100 | | | ns |
| SCLK Pulse Width High | tCH | | 40 | | | ns |
| SCLK Pulse Width Low | tCL | | 40 | | | ns |
| \overline{CS} Fall to SCLK Rise Setup Time | tCSS | | 40 | | | ns |
| SCLK Rise to \overline{CS} Rise Hold Time | tCSH | | 0 | | | ns |
| DIN Setup Time | tDS | | 40 | | | ns |
| DIN Hold Time | tDH | | 0 | | | ns |
| SCLK Rise to \overline{CS} Fall Delay | tCS0 | | 40 | | | ns |
| \overline{CS} Rise to SCLK Rise Hold Time | tCS1 | | 40 | | | ns |
| \overline{CS} Pulse Width High | tCSW | | 100 | | | ns |

Note 1: Guaranteed from code 3 to code 1023 in unity-gain configuration.

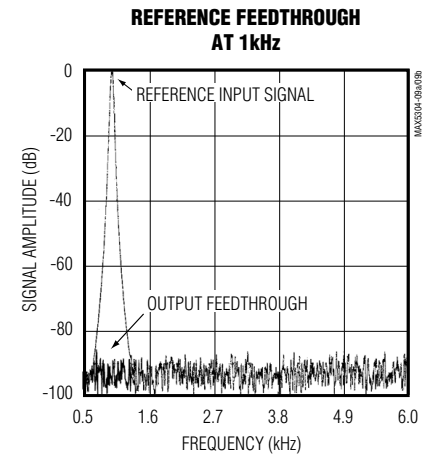
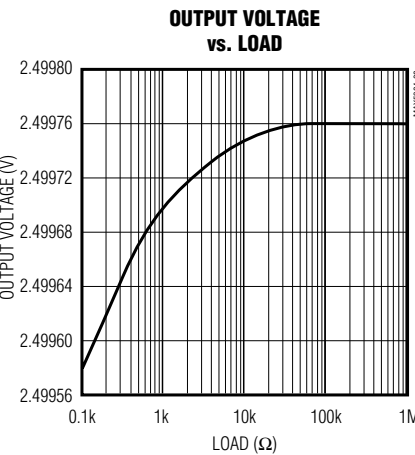
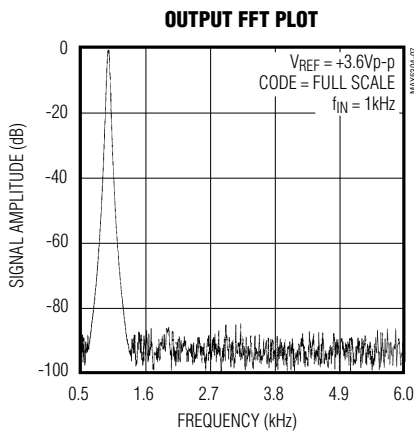
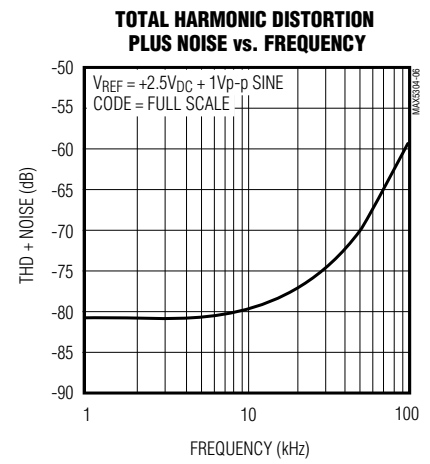
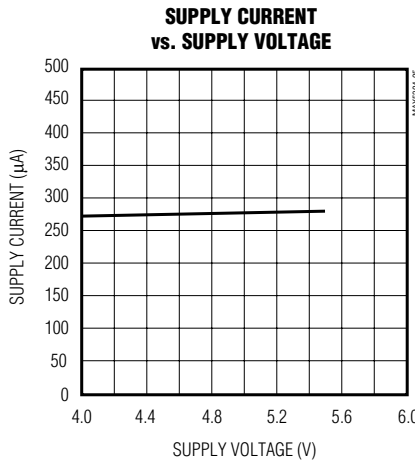
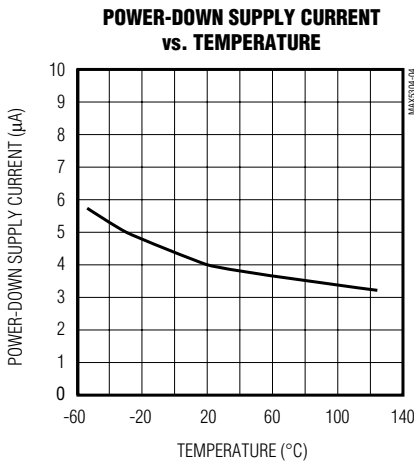
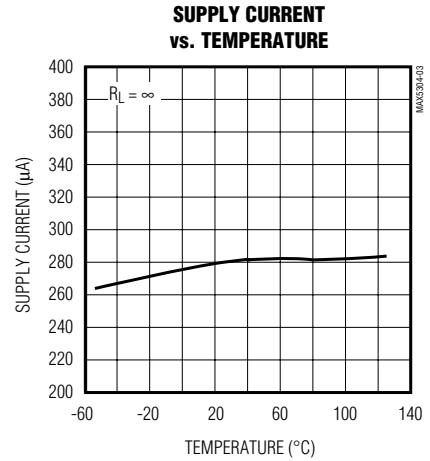
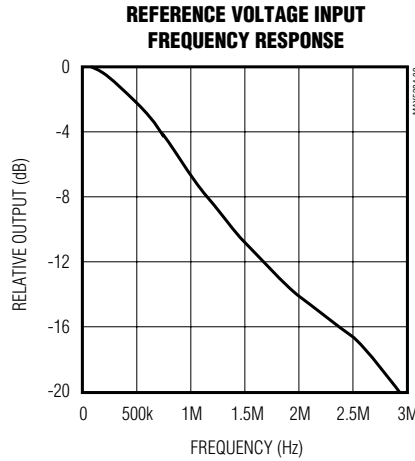
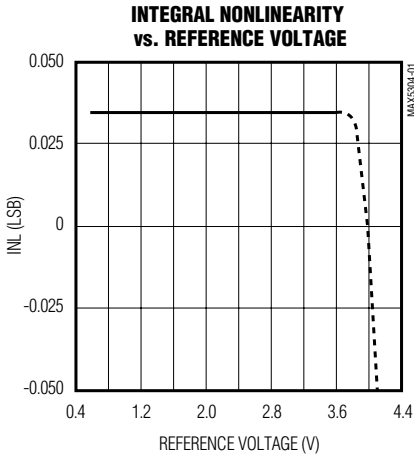
Note 2: Accuracy is better than 1LSB for $V_{OUT} = 8mV$ to $(V_{DD} - 100mV)$, guaranteed by a power-supply rejection test at the end points.

Note 3: $R_L = \infty$, digital inputs at GND or V_{DD} .

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Typical Operating Characteristics

($V_{DD} = +5V$, $R_L = 5k\Omega$, $C_L = 100pF$, $T_A = +25^\circ C$, unless otherwise noted.)

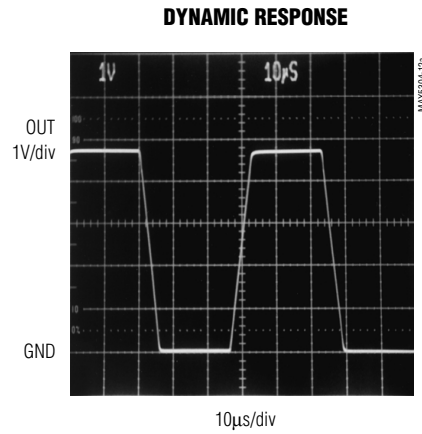
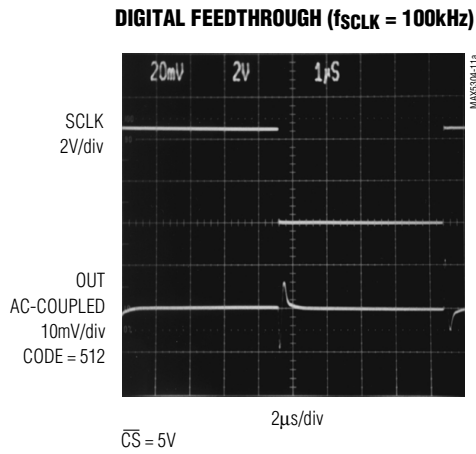
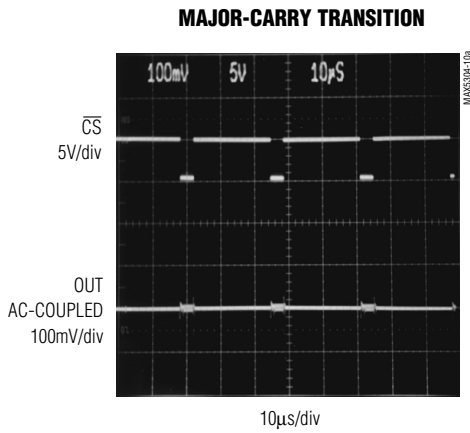


10-Bit Voltage-Output DAC in 8-Pin μ MAX

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Typical Operating Characteristics (continued)

($V_{DD} = +5V$, $R_L = 5k\Omega$, $C_L = 100pF$, $T_A = +25^\circ C$, unless otherwise noted.)



GAIN = +2V/V, SWITCHING FROM CODE 0 TO 1005

10-Bit Voltage-Output DAC in 8-Pin μ MAX

Pin Description

| PIN | NAME | FUNCTION |
|-----|------------------------|--------------------------------|
| 1 | OUT | DAC Output Voltage |
| 2 | $\overline{\text{CS}}$ | Chip-Select Input. Active low. |
| 3 | DIN | Serial-Data Input |
| 4 | SCLK | Serial-Clock Input |
| 5 | FB | DAC Output Amplifier Feedback |
| 6 | REF | Reference Voltage Input |
| 7 | GND | Ground |
| 8 | V _{DD} | Positive Power Supply |

Detailed Description

The MAX5304 contains a voltage-output digital-to-analog converter (DAC) that is easily addressed using a simple 3-wire serial interface. Each IC includes a 16-bit shift register, and has a double-buffered input composed of an input register and a DAC register (see the *Functional Diagram*). In addition to the voltage output, the amplifier's negative input is available to the user.

The DAC is an inverted R-2R ladder network that converts a digital input (10 data bits plus 3 sub-bits) into an equivalent analog output voltage in proportion to the applied reference voltage. Figure 1 shows a simplified circuit diagram of the DAC.

Reference Inputs

The reference input accepts positive DC and AC signals. The voltage at the reference input sets the full-scale output voltage for the DAC. The reference input voltage range is 0V to (V_{DD} - 1.4V). The output voltage (V_{OUT}) is represented by a digitally programmable voltage source, as expressed in the following equation:

$$V_{\text{OUT}} = (V_{\text{REF}} \cdot \text{NB} / 1024) \text{ Gain}$$

where NB is the numeric value of the DAC's binary input code (0 to 1023), V_{REF} is the reference voltage, and Gain is the externally set voltage gain.

The impedance at the reference input is code dependent, ranging from a low value of 18k Ω when the DAC has an input code of 1550 hex, to a high value exceeding several gigohms (leakage currents) with an input code of 0000 hex. Because the input impedance at the reference pin is code dependent, load regulation of the reference source is important.

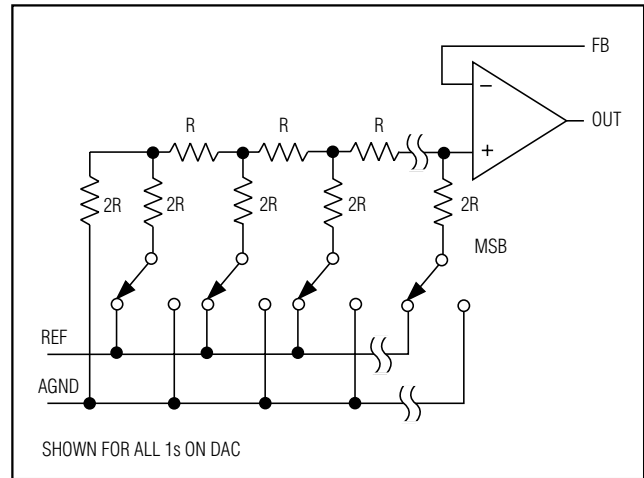


Figure 1. Simplified DAC Circuit Diagram

In shutdown mode, the MAX5304's REF input enters a high-impedance state with a typical input leakage current of 0.001 μ A.

The reference input capacitance is also code dependent and typically ranges from 15pF (with an input code of all 0s) to 50pF (at full scale).

The MAX873 +2.5V reference is recommended for use with the MAX5304.

Output Amplifier

The MAX5304's DAC output is internally buffered by a precision amplifier with a typical slew rate of 0.6V/ μ s. Access to the output amplifier's inverting input provides the user greater flexibility in output gain setting/signal conditioning (see the *Applications Information* section).

With a full-scale transition at the MAX5304 output, the typical settling time to $\pm 1/2$ LSB is 10 μ s when loaded with 5k Ω in parallel with 100pF (loads less than 2k Ω degrade performance).

The amplifier's output dynamic responses and settling performances are shown in the *Typical Operating Characteristics*.

Shutdown Mode

The MAX5304 features a software-programmable shutdown that reduces supply current to a typical value of 4 μ A. Writing 111X XXXX XXXX XXXX as the input-control word puts the device in shutdown mode (Table 1).

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In shutdown mode, the amplifier's output and the reference input enter a high-impedance state. The serial interface remains active. Data in the input register is retained in shutdown, allowing the MAX5304 to recall the output state prior to entering shutdown. Exit shutdown mode by either recalling the previous configuration or updating the DAC with new data. When powering up the device or bringing it out of shutdown, allow 20 μ s for the outputs to stabilize.

Serial-Interface Configurations

The MAX5304's 3-wire serial interface is compatible with MICROWIRE (Figure 2) and SPI/QSPI (Figure 3). The serial-input word consists of three control bits followed by 10+3 data bits (MSB first), as shown in Figure 4. The 3-bit control code determines the MAX5304's response outlined in Table 1.

The MAX5304's digital inputs are double buffered. Depending on the command issued through the serial interface, the input register can be loaded without affecting the DAC register, the DAC register can be loaded directly, or the DAC register can be updated from the input register (Table 1).

Serial-Interface Description

The MAX5304 requires 16 bits of serial data. Table 1 lists the serial-interface programming commands. For certain commands, the 10+3 data bits are "don't cares." Data is sent MSB first and can be sent in two 8-bit packets or one 16-bit word (\overline{CS} must remain low until 16 bits are transferred). The serial data is composed of three control bits (C2, C1, C0), followed by the 10+3 data bits D9...D0, S2, S1, S0 (Figure 4). Set the sub-bits (S2, S1, S0) to zero. The 3-bit control code determines the register to be updated and the configuration when exiting shutdown.

Figure 5 shows the serial-interface timing requirements. The chip-select pin (\overline{CS}) must be low to enable the DAC's serial interface. When \overline{CS} is high, the interface control circuitry is disabled. \overline{CS} must go low at least t_{CSS} before the rising serial-clock (SCLK) edge to properly clock in the first bit. When \overline{CS} is low, data is clocked into the internal shift register through the serial-data input pin (DIN) on SCLK's rising edge. The maximum guaranteed clock frequency is 10MHz. Data is latched into the MAX5304 input/DAC register on \overline{CS} 's rising edge.

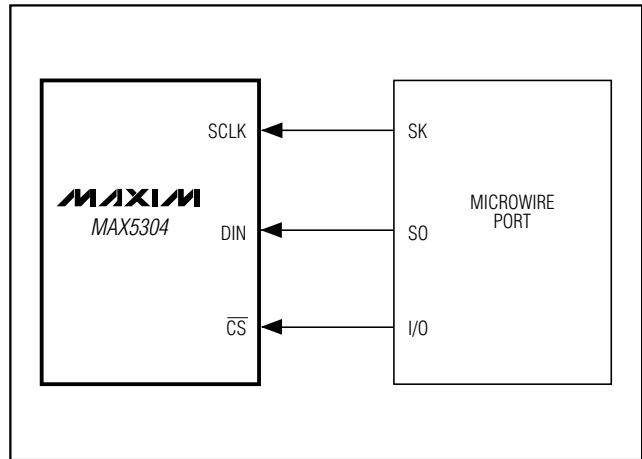


Figure 2. Connections for MICROWIRE

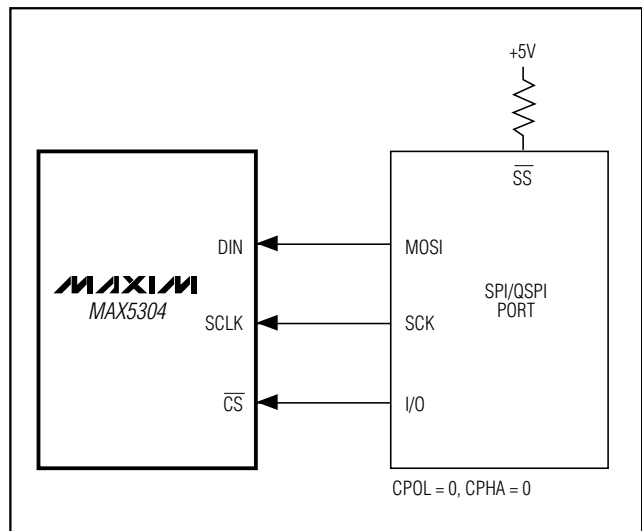


Figure 3. Connections for SPI/QSPI

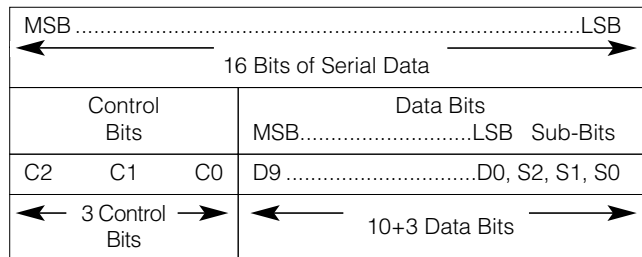


Figure 4. Serial-Data Format

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Table 1. Serial-Interface Programming Commands

| 16-BIT SERIAL WORD | | | | | FUNCTION |
|--------------------|----|----|---|---------|--|
| C2 | C1 | C0 | D9.....D0 MSB LSB | S2...S0 | |
| X | 0 | 0 | 10 bits of data | 000 | Load input register; DAC register immediately updated (also exit shutdown). |
| X | 0 | 1 | 10 bits of data | 000 | Load input register; DAC register unchanged. |
| X | 1 | 0 | XXXXXXXXXX | XXX | Update DAC register from input register (also exit shutdown; recall previous state). |
| 1 | 1 | 1 | XXXXXXXXXX | XXX | Shutdown |
| 0 | 1 | 1 | XXXXXXXXXX | XXX | No operation (NOP) |

X = Don't care

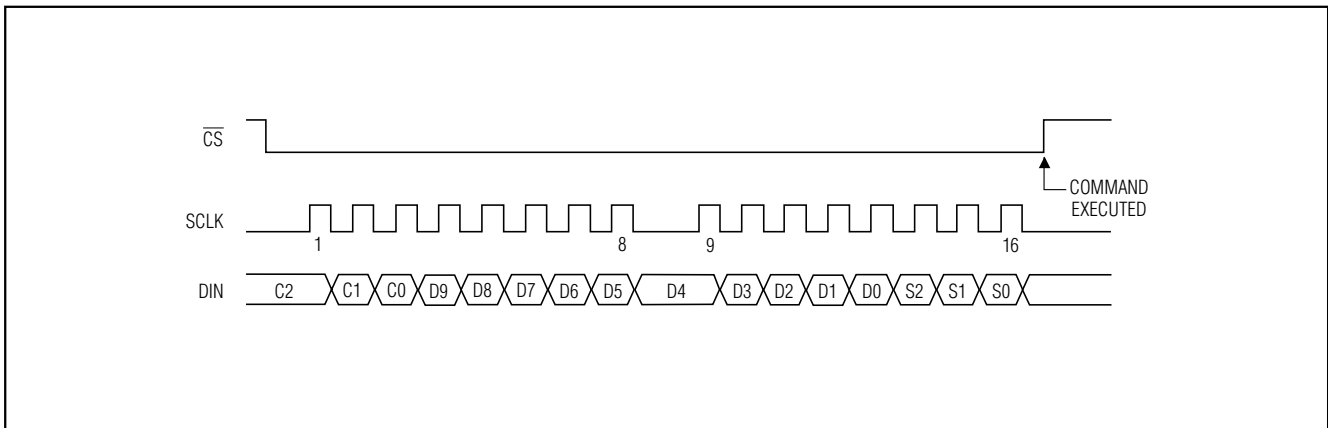


Figure 5. Serial-Interface Timing Diagram

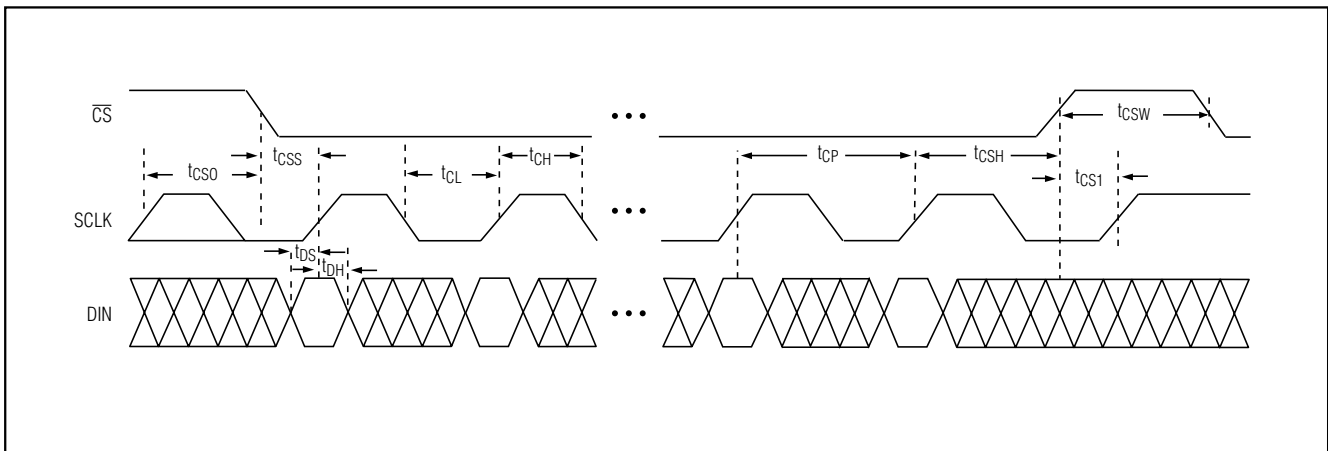


Figure 6. Detailed Serial-Interface Timing Diagram

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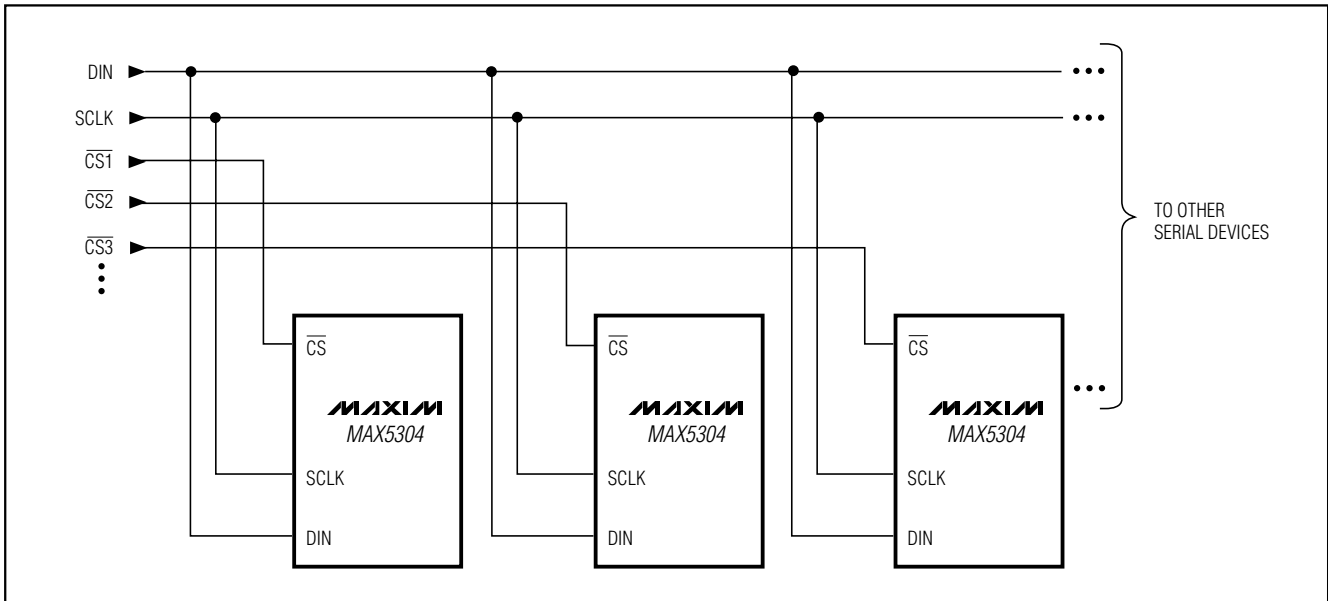


Figure 7. Multiple MAX5304s Sharing Common DIN and SCLK Lines

Figure 7 shows a method of connecting several MAX5304s. In this configuration, the clock and the data bus are common to all devices, and separate chip-select lines are used for each IC.

Applications Information

Unipolar Output

For a unipolar output, the output voltage and the reference input have the same polarity. Figure 8 shows the MAX5304 unipolar output circuit, which is also the typical operating circuit. Table 2 lists the unipolar output codes.

Figure 9 illustrates a Rail-to-Rail[®] output configuration. This circuit shows the MAX5304 with the output amplifier configured for a closed-loop gain of $+2V/V$ to provide a 0 to 5V full-scale range when a 2.5V reference is used.

Bipolar Output

The MAX5304 output can be configured for bipolar operation using Figure 10's circuit according to the following equation:

$$V_{OUT} = V_{REF} [(2NB / 1024) - 1]$$

where NB is the numeric value of the DAC's binary input code. Table 3 shows digital codes (offset binary) and corresponding output voltages for Figure 10's circuit.

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

Table 2. Unipolar Output Codes

| DAC CONTENTS | | ANALOG OUTPUT |
|--------------|-----------------|---|
| MSB | LSB | |
| 11 | 1111 1111 (000) | $+V_{REF} \left(\frac{1023}{1024} \right)$ |
| 10 | 0000 0001 (000) | $+V_{REF} \left(\frac{513}{1024} \right)$ |
| 10 | 0000 0000 (000) | $+V_{REF} \left(\frac{512}{1024} \right) = \frac{+V_{REF}}{2}$ |
| 01 | 1111 1111 (000) | $+V_{REF} \left(\frac{511}{1024} \right)$ |
| 00 | 0000 0001 (000) | $+V_{REF} \left(\frac{1}{1024} \right)$ |
| 00 | 0000 0000 (000) | 0V |

Note: () are for sub-bits.

Using an AC Reference

In applications where the reference has AC signal components, the MAX5304 has multiplying capability within the reference input range specifications. Figure 11 shows a technique for applying a sine-wave signal to the reference input where the AC signal is offset before being applied to REF. The reference voltage must never be more negative than GND.

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Table 3. Bipolar Output Codes

| DAC CONTENTS | | ANALOG OUTPUT |
|--------------|-----------------|--|
| MSB | LSB | |
| 11 | 1111 1111 (000) | $+V_{REF} \left(\frac{511}{512} \right)$ |
| 10 | 0000 0001 (000) | $+V_{REF} \left(\frac{1}{512} \right)$ |
| 10 | 0000 0000 (000) | 0V |
| 01 | 1111 1111 (000) | $-V_{REF} \left(\frac{1}{512} \right)$ |
| 00 | 0000 0001 (000) | $-V_{REF} \left(\frac{511}{512} \right)$ |
| 00 | 0000 0000 (000) | $-V_{REF} \left(\frac{512}{512} \right) = -V_{REF}$ |

Note: () are for sub-bits.

The MAX5304's total harmonic distortion plus noise (THD+N) is typically less than -77dB (full-scale code), given a 1Vp-p signal swing and input frequencies up to 25kHz. The typical -3dB frequency is 650kHz, as shown in the *Typical Operating Characteristics* graphs.

Digitally Programmable Current Source

Figure 12's circuit places an NPN transistor (2N3904 or similar) within the op amp feedback loop to implement a digitally programmable, unidirectional current source. The output current is calculated with the following equation:

$$I_{OUT} = (V_{REF} / R)(NB / 1024)$$

where NB is the numeric value of the DAC's binary input code, and R is the sense resistor shown in Figure 12.

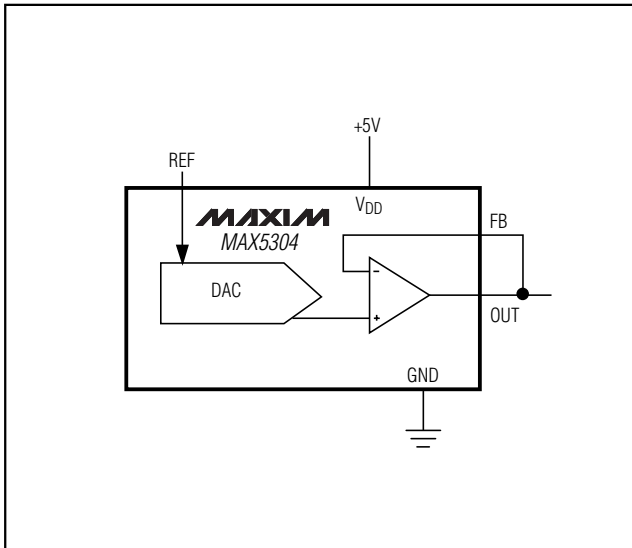


Figure 8. Unipolar Output Circuit

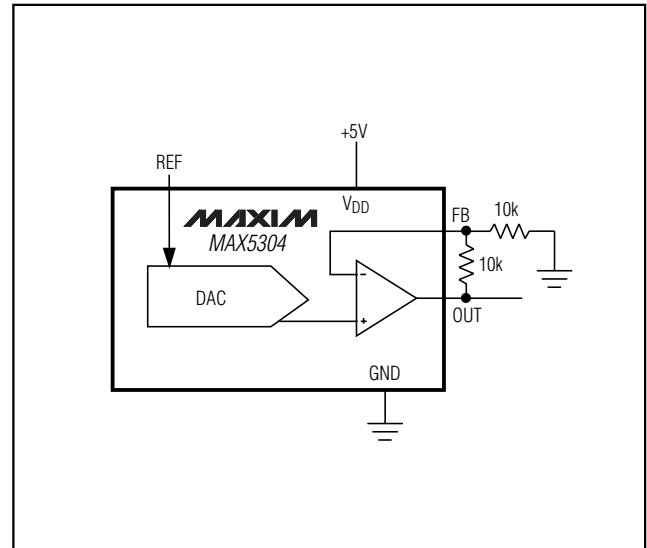


Figure 9. Unipolar Rail-to-Rail Output Circuit

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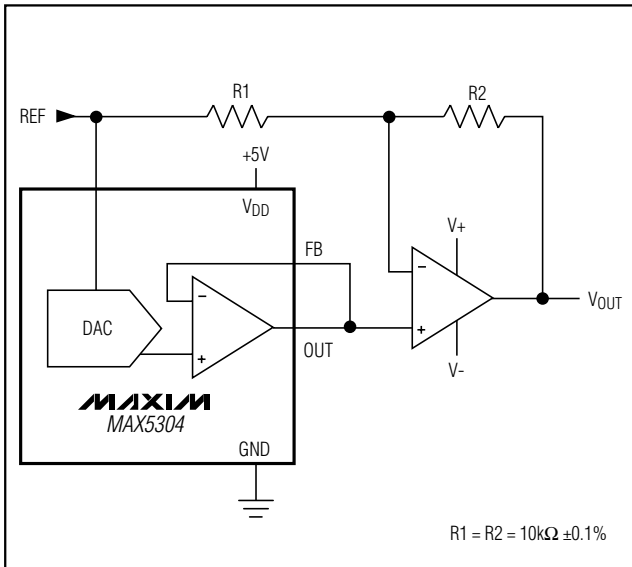


Figure 10. Bipolar Output Circuit

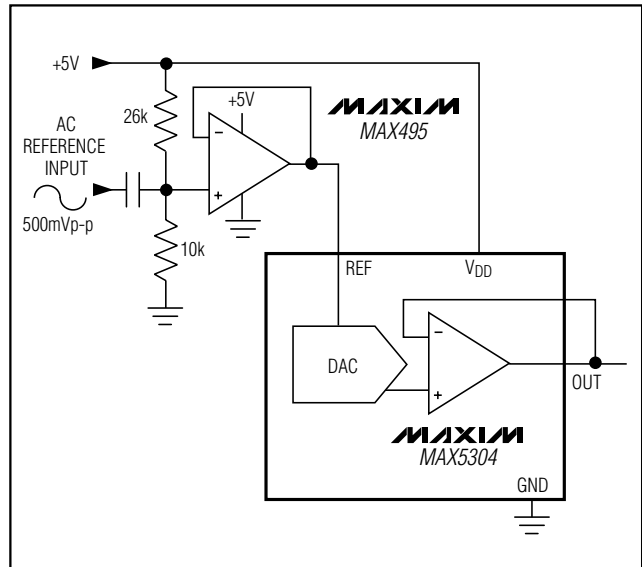


Figure 11. AC Reference Input Circuit

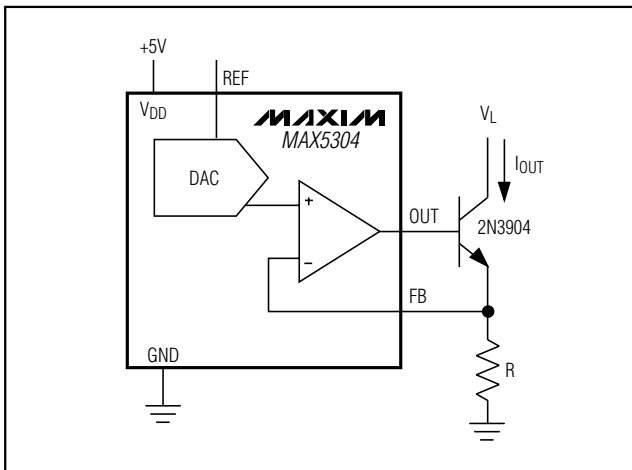


Figure 12. Digitally Programmable Current Source

Power-Supply Considerations

On power-up, the input and DAC registers are cleared (set to zero code). For rated MAX5304 performance, REF must be at least 1.4V below VDD. Bypass VDD with a 4.7 μ F capacitor in parallel with a 0.1 μ F capacitor to GND. Use short lead lengths, and place the bypass capacitors as close to the supply pins as possible.

Grounding and Layout Considerations

Digital or AC transient signals on GND can create noise at the analog output. Connect GND to the highest-quality ground available. Good PC board ground layout minimizes crosstalk between the DAC output, reference input, and digital input. Reduce crosstalk by keeping analog lines away from digital lines. Wire-wrapped boards are not recommended.

Chip Information

TRANSISTOR COUNT: 3053

SUBSTRATE CONNECTED TO AGND

10-Bit Voltage-Output DAC in 8-Pin μ MAX

Package Information

8LUMAXDEPS

TOP VIEW

BOTTOM VIEW

FRONT VIEW

SIDE VIEW

| | INCHES | | MILLIMETERS | | JEDEC | | | |
|----------|--------|-------|-------------|-------|--------|-------|------|------|
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX |
| A | 0.037 | 0.043 | 0.94 | 1.10 | --- | 0.043 | --- | 1.10 |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 |
| B | 0.010 | 0.014 | 0.25 | 0.36 | 0.010 | 0.016 | 0.25 | 0.40 |
| C | 0.005 | 0.007 | 0.13 | 0.18 | 0.005 | 0.009 | 0.13 | 0.23 |
| D | 0.116 | 0.120 | 2.95 | 3.05 | 0.114 | 0.122 | 2.9 | 3.1 |
| e | 0.0256 | BSC | 0.65 | BSC | 0.0256 | BSC | 0.64 | BSC |
| E | 0.116 | 0.120 | 2.95 | 3.05 | 0.114 | 0.122 | 2.9 | 3.1 |
| H | 0.188 | 0.198 | 4.78 | 5.03 | 0.193 | BSC | 4.9 | BSC |
| L | 0.016 | 0.026 | 0.41 | 0.66 | 0.016 | 0.027 | 0.40 | 0.70 |
| α | 0° | 6° | 0° | 6° | 0° | 6° | 0° | 6° |
| *X | 0.087 | 0.099 | 2.210 | 2.515 | | | | |
| *Y | 0.062 | 0.074 | 1.575 | 1.880 | | | | |

* EXPOSED PAD

NOTES:
 1. D&E DO NOT INCLUDE MOLD FLASH.
 2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 MM (.006").
 3. CONTROLLING DIMENSION: MILLIMETERS.
 4. MEETS JEDEC MO-187.
 5. DIMENSIONS X & Y APPLY TO EXPOSED PAD VERSIONS ONLY.
 6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM

PROPRIETARY INFORMATION

TITLE:
PACKAGE OUTLINE, 8L μ MAX

| | | |
|----------|----------------------|-------|
| APPROVAL | DOCUMENT CONTROL NO. | REV |
| | 21-0036 | G 1/1 |

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